

# 31 Election  
OKing  
10/12/01

PATENT APPLICATION



In re application of

Kaoru NARITA

Appln. No.: 09/421,273

Group Art Unit: 2823

Confirmation No.: (not yet assigned)

Examiner: J. Garcia

Filed: October 20, 1999

For: SEMICONDUCTOR DEVICE HAVING  
PROTECTION CIRCUIT IMPLEMENTED BY  
BIPOLAR TRANSISTOR FOR DISCHARGING  
STATIC CHARGE CURRENT AND PROCESS  
OF FABRICATION

RECEIVED  
OCT 10 2001  
Group 2100

RESPONSE TO RESTRICTION REQUIREMENT

Commissioner for Patents  
Washington, D.C. 20231

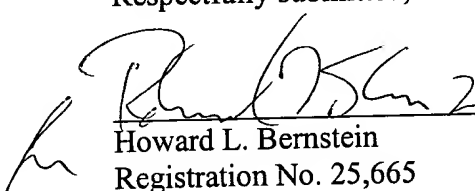
Sir:

In response to the Office Action dated September 11, 2001, in which the Examiner has required a restriction, Applicant responds by electing Group I, *i.e.*, claims 1-15, drawn to a device. This election is made without prejudice to the filing of a divisional application directed to the non-elected claims.

Prompt and favorable action on the elected claims is now respectfully requested.

Respectfully submitted,

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Howard L. Bernstein  
Registration No. 25,665

Date: October 5, 2001

TECHNICAL/REGISTRATION SECTION  
OCT 11 2001  
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